STUDY OF
SHORT TERM PHASE STABILITY

SMITH ELECTRONICS, INC
Cleveland 41, Ohio

FINAL REPORT

September 17, 1966
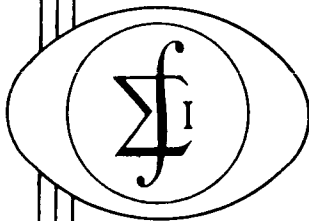
CONTRACT NO NAS 8-11592

MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

FINAL REPORT

STUDY OF SHORT-TERM PHASE STABILITY

CONTRACT NAS 8-11592

September 6, 1965 - September 17, 1966

September 17, 1966

Prepared for:

George C. Marshall Space Flight Center
National Aeronautics & Space Administration
Huntsville, Alabama

Report prepared by: *Robert A. Mostrom*

Robert A. Mostrom, Project Engineer

CONTENTS

FIGURES

SMITH ELECTRONICS, INC.

ABSTRACT

12253

Theoretical and experimental work is described leading to the conclusion that at least two mechanisms may be present in subharmonic generators employing charge-storage diodes. One is the generation of negative resistance by a parametric mode of operation; the other is a coincidence and timing mode relating to the abrupt transition phenomenon.

Development of a coherent fractional frequency multiplier employing charge-storage diodes in harmonic and subharmonic operation exclusively is also described.

A review of selected short-term stability measurement systems is presented, including a description of a phase comparator system employed by the contractor.

Author

STUDY OF SHORT-TERM STABILITY

Final Report covering work done on Contract NAS 8-11592
during the Period September 6, 1965 - September 17, 1965.

I. INTRODUCTION

Since March 16, 1964, Smith Electronics, Inc. has conducted
investigations in the general area of short-term stability, including phase-
stable devices, under Contract NAS 8-11592. An interim report was issued
in March 1965 covering work done in the period March 16, 1964 through
March 16, 1965. A second interim report covered the period March 17,
1965 through September 5, 1965. The current report, covering September
6, 1965 through September 17, 1966, describes work which was carried on
in two major areas. The first was a study of frequency division, consisting
of theoretical and experimental phases. The second was a review of the
theory and instrumentation for measurement of phase stability.

The study of frequency division was particularly oriented toward
the charge-storage diode subharmonic generator. It resulted in better
understanding of the mechanisms involved, through both theoretical and
experimental investigations. A specific objective of the contract was the
development of a coherent fractional frequency multiplier using step-re-
covery diode frequency changers. The successful accomplishment of this
objective contributed much to the practical understanding of the step-re-
covery frequency divider.

The phase stability instrumentation phase of the program in-
cluded a re-assessment of currently used methods. The phase comparator
system used at SEI was found to be a useful procedure, and the significance
of its readout was investigated.

II. STUDY OF FREQUENCY DIVISION

Earlier work on the subject contract demonstrated the usefulness
of the charge-storage diode as a high-efficiency subharmonic generator.
This work was continued and expanded in both thoeretical and practical areas.

A. Theory

The theoretical study of the charge-storage frequency divider was undertaken to improve insight into circuit action for the purpose of 1) improving the dividers further, and 2) understanding the potential capabilities of such frequency changers. Early in the study, it became apparent that the non-linear and time-dependent nature of the charge-storage diode made a closed form analytical solution unattainable. It had been hoped that the analysis would supply information on input and output coupling, impedance levels and Q's. The optimum idler configuration or combinations of idlers was to have been determined.

The analytical methods examined included direct solution of the equations, transform solutions and piecewise solutions. None of these were productive. The most useful paper work was a graphic solution with an arbitrarily constrained diode. In this study, several different subharmonic cases were considered with appropriate idlers. In each case, by summing the waveforms due to input idler and output signals, it was shown that the resultant voltage across the step-recovery diode was such as to produce coincidence with the diode transition in such a phase relationship as to sustain operation. In certain cases, it was observed that proper biasing would be required for operation to occur.

Measurements were made on step-recovery diodes of the types being used for the experimental program (Para. B). These showed appreciably higher resistive components than commonly reported. Where resistances in the vicinity of 5 ohms are considered typical, these measurements showed 50 to 80 ohms could be expected. Figure 1 is a Smith chart plot of measured values with various dc bias levels.

An analysis based on the diode dc resistance and switched-on, switched-off ratio indicated that the higher values are not unreasonable. Moreover, analysis of matching networks used in practical circuits tended to confirm the higher values.

A solution of the subharmonic generator circuit using a computer analysis has been suggested in earlier reports. Also, the analog circuit

Z_0	Y_0	TITLE	DWG. NO.	382A
50 Ω		FIG. 1 Step-Recovery Diode	DATE	660916

Impedance vs Bias

IMPEDANCE OR ADMITTANCE COORDINATES

MA 4754
Step-Recovery
Diode

1 GHz
1 kHz Mod.

40 μα
30 μα
25 μα
15 μα
20 μα
0 μα
10 μα
2.5 μα
5 μα

Smith Electronics, Inc., Cleveland, Ohio

RADIALLY SCALED PARAMETERS

TOWARD GENERATOR ——→   ←—— TOWARD LOAD

CENTER
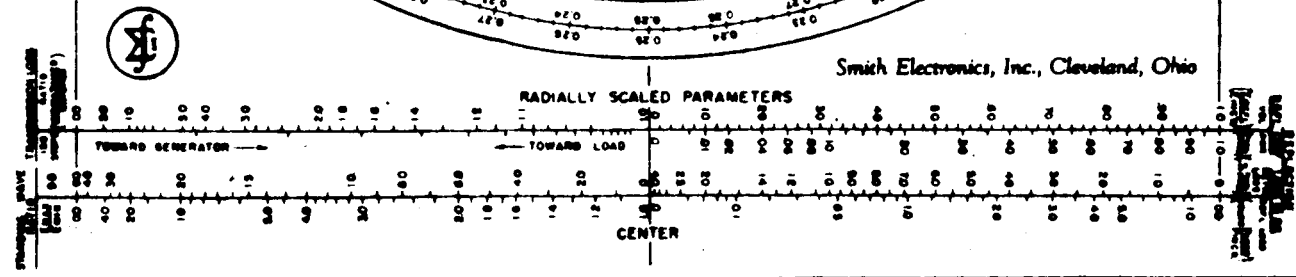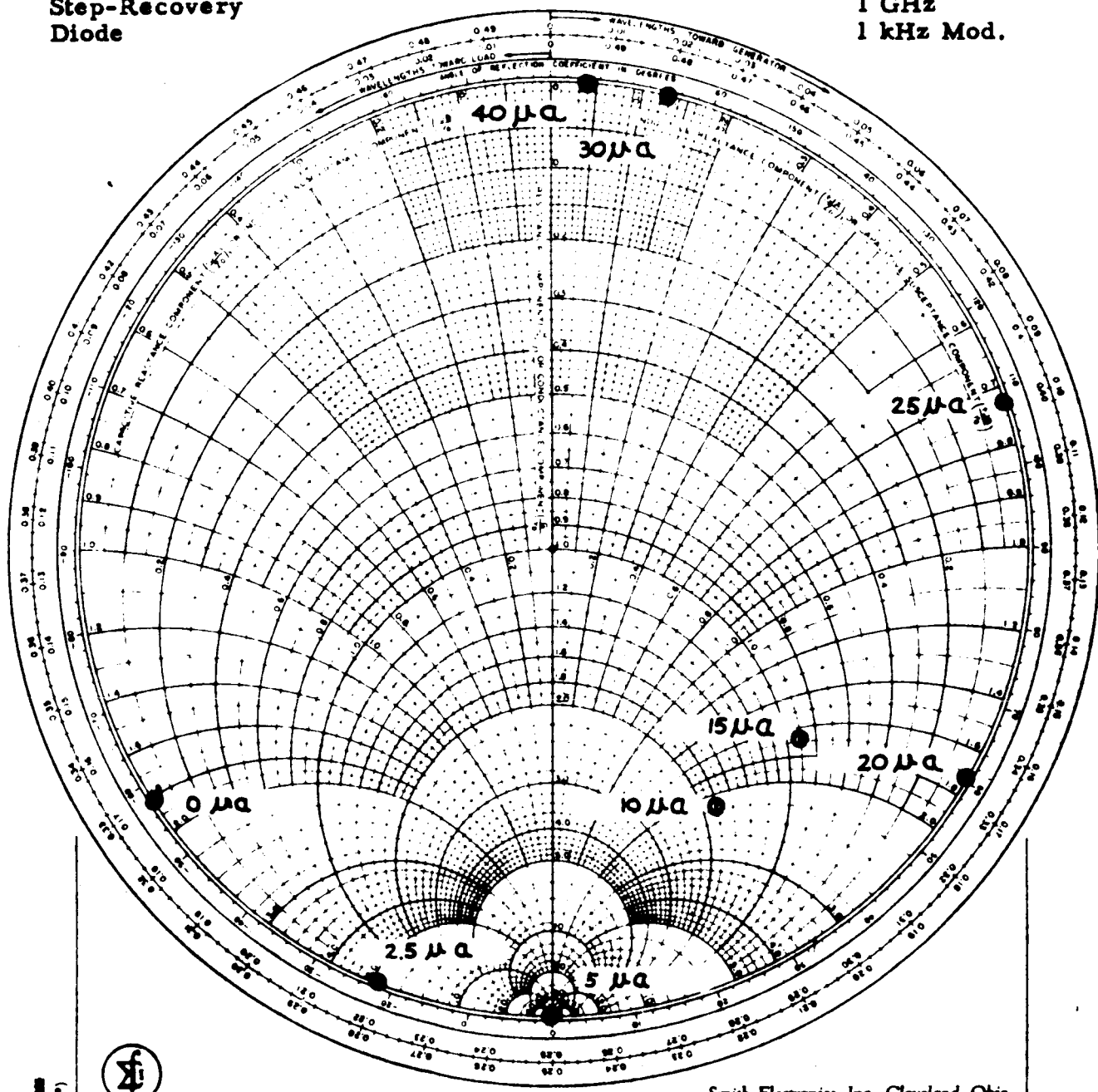
proposed in the interim report dated September 6, 1965, capable of synthesizing the step-recovery diode waveform at audio frequencies, still appears to be a valuable tool for understanding the frequency-changing mechanisms. Probably, the computer solution would be most useful for parametric studies.

B. Coherent Fractional Frequency Multiplier

A specific objective of the subject contract was the development of a coherent fractional frequency multiplier capable of delivering a 2282.5 MHz signal from an input of 2101.8 MHz, or a 240/221 ratio of output to input signals. This task was successfully completed and one experimental unit delivered to MSFC on June 10, 1966. A special report covering this development has been issued. Therefore, the subject will be treated here in condensed form.

1) Significance of Phase Coherence

Concurrently with the development of the fractional frequency multiplier, the concept of coherence was reviewed. Coherence of two signals at the same frequency is a concept readily understood. However, when the two signals are of different frequencies, particularly when non-harmonically related, the significance of coherence is less clear.

Basically, coherence implies that at any time either signal can be specified deterministically (rather than statistically) in terms of the other. Qualitatively, this means for signals of different frequencies that there will be a certain period at which recognizable patterns of correspondence between the two signals will repeat.

If phase coherence exists between two signals, however distorted or noisy they may be, there will be one sine or cosine wave from each signal demonstrating the above pattern of correspondence. Let the two signals be

$$Y_1(t) = A \sin \omega_1 t \tag{1}$$

$$Y_2(t) = B \sin \omega_2 t \tag{2}$$

where

ω_2 is the higher frequency.

Then the period at which the pattern of correspondence repeats (if it exists) will be given by

$$p = 2\pi n_1/\omega_1 = 2\pi n_2/\omega_2 \tag{3}$$

where

n_2/n_1 is ω_2/ω_1 reduced to lowest terms.

2) Device Development

The philosophy employed as well as the results achieved with the fractional frequency multiplier are shown in the block diagram of Fig. 2. Two frequency dividers and two multipliers are employed, each using step-recovery diodes. Two transistor amplifiers provide sufficient gain to compensate for losses and to permit operation of the stages at optimum levels.

The dividers are modifications of the three-frequency type described in the Interim Report dated September 6, 1965. A tuned idler circuit at a frequency (n - 1) f, where f is the output frequency and nf is the input, is used. Improved idler circuitry and a phase adjustment circuit result in excellent stability, efficiency and operational bandwidth.

The step-recovery multiplier stages are straightforward, with reasonably good efficiency, bandwidth and stability.

Figures 3, 4 and 5 show typical circuitry employed in the modules, and Fig. 6 shows the completed assembly.

The overall system bandwidth and dynamic range are such as to permit frequency modulation of the input signal ± 1.84 MHz over an input level range of 3 dB.

Phase stability measurements were made using two complete and nearly identical chains in a phase comparator setup. The measured RMS phase jitter was 3.1×10^{-3} radians.
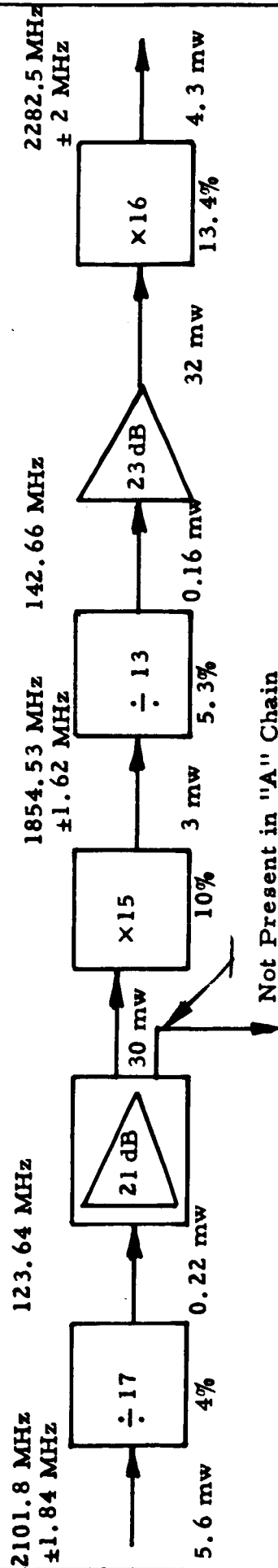
329-A

FIG. 2 COHERENT FRACTIONAL FREQUENCY MULTIPLIER

"A" CHAIN APPROXIMATE MEASURED LEVELS

326 A

123.64 MHs

2101.8 MHs

MA 4754
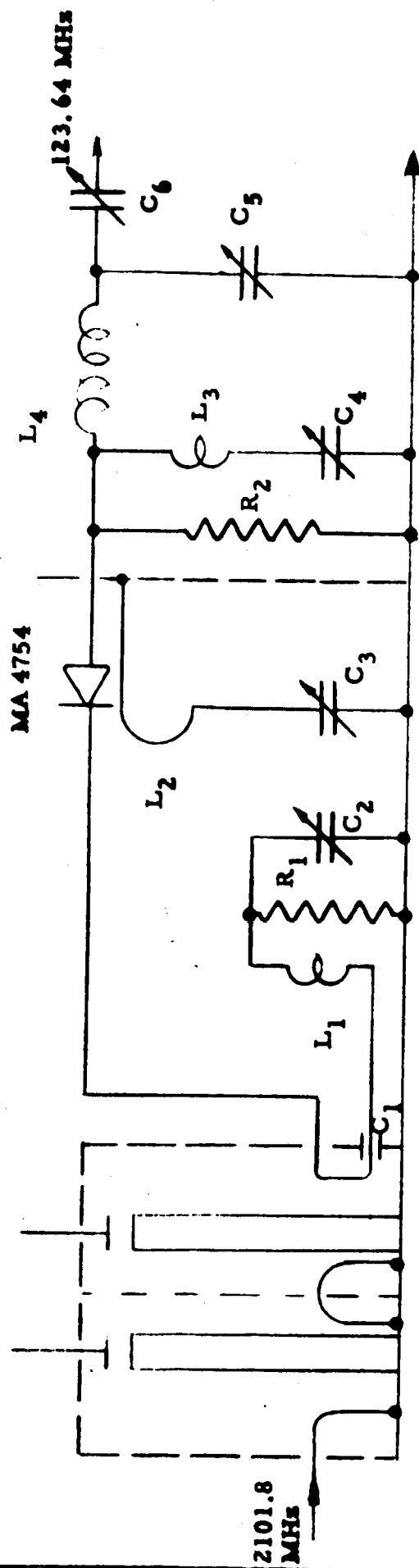
FIG. 3   SCHEMATIC OF ÷ 17 STAGE

123.64 MHz

MA 4754

1854.53 MHz
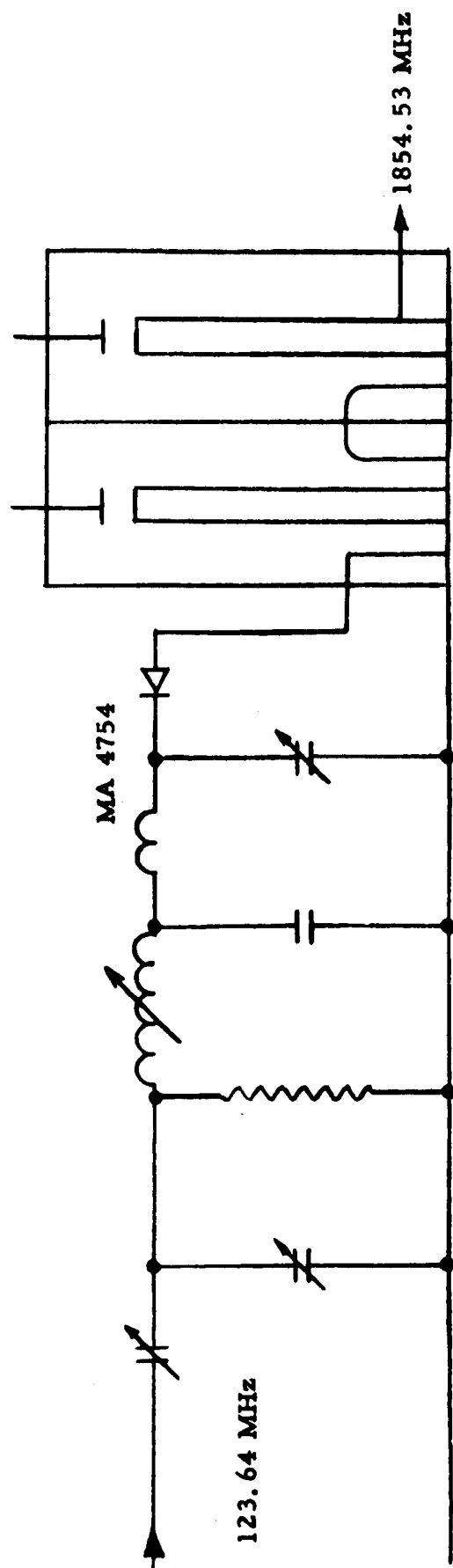
FIG. 4   ×15 MULTIPLIER STAGE
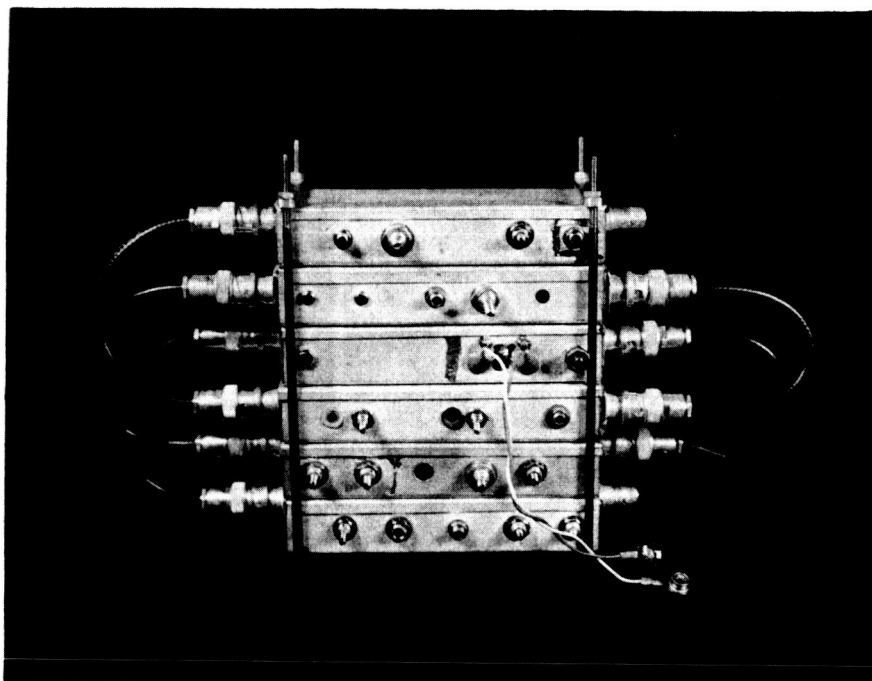
200A
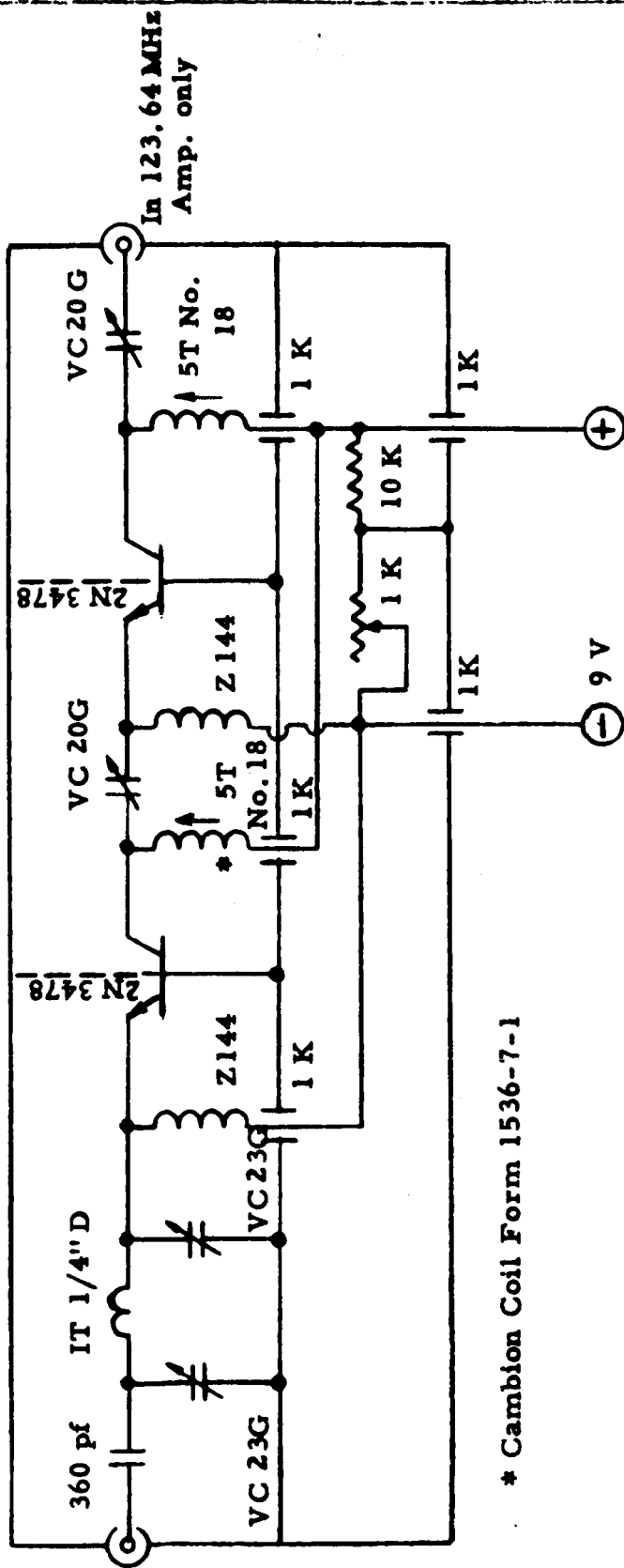
FIG. 5   142.6 MHz AMPLIFIER

FIG. 6   COHERENT FRACTIONAL FREQUENCY
MULTIPLIER "A" CHAIN ASSEMBLED

C.   Other Experimental Work

The block diagram of the fractional frequency multiplier, Fig. 2, shows an additional output at 123.64 MHz. It was planned to use another ÷ 13 module to obtain 9.51 MHz from this port.   Circuits for this function using step-recovery diodes were fabricated and tested.   No truly successful results were achieved, although some interesting and illuminating observations were made.   For example, when pumped at 123.64 MHz, the step-recovery diode readily generated very strong oscillations at or near the frequency of the 9.51 MHz output resonator. With careful tuning, some small degree of locking at the subharmonic frequency was achieved.   However, the behavior was more generally characterized by a free oscillation, the frequency of which was determined more by resonator tuning than by subharmonic considerations. This behavior had been observed with the UHF dividers, but never as spectacularly. It seems to indicate that negative resistance can easily be generated in charge-storage circuits at frequencies other than the pump frequency. Moreover, these observations further reinforce the belief that negative resistance plays an important part in subharmonic generation, and that the subharmonic output may be an oscillation which is phase locked harmonically to the input and idler frequencies.

Figure 7 shows schematically an experimental setup which was fabricated for the purpose of isolating and identifying the contribution of the three significant frequencies in subharmonic generation.   No experimental results were obtained because the approaching termination of the contract period required that efforts be concentrated elsewhere.

D.   Conclusions

The theoretical and experimental programs seem to justify the following observations with respect to step-recovery diode subharmonic generators of the type studied:

1)   It is likely more than one mechanism is involved in subharmonic generation.

2)   Negative resistance oscillations apparently are readily generated at or near subharmonic frequencies.   This mode may make use of the abrupt charge-voltage non-linearity approximating the behavior of an ideal varactor.

332 A

575
MHz

in

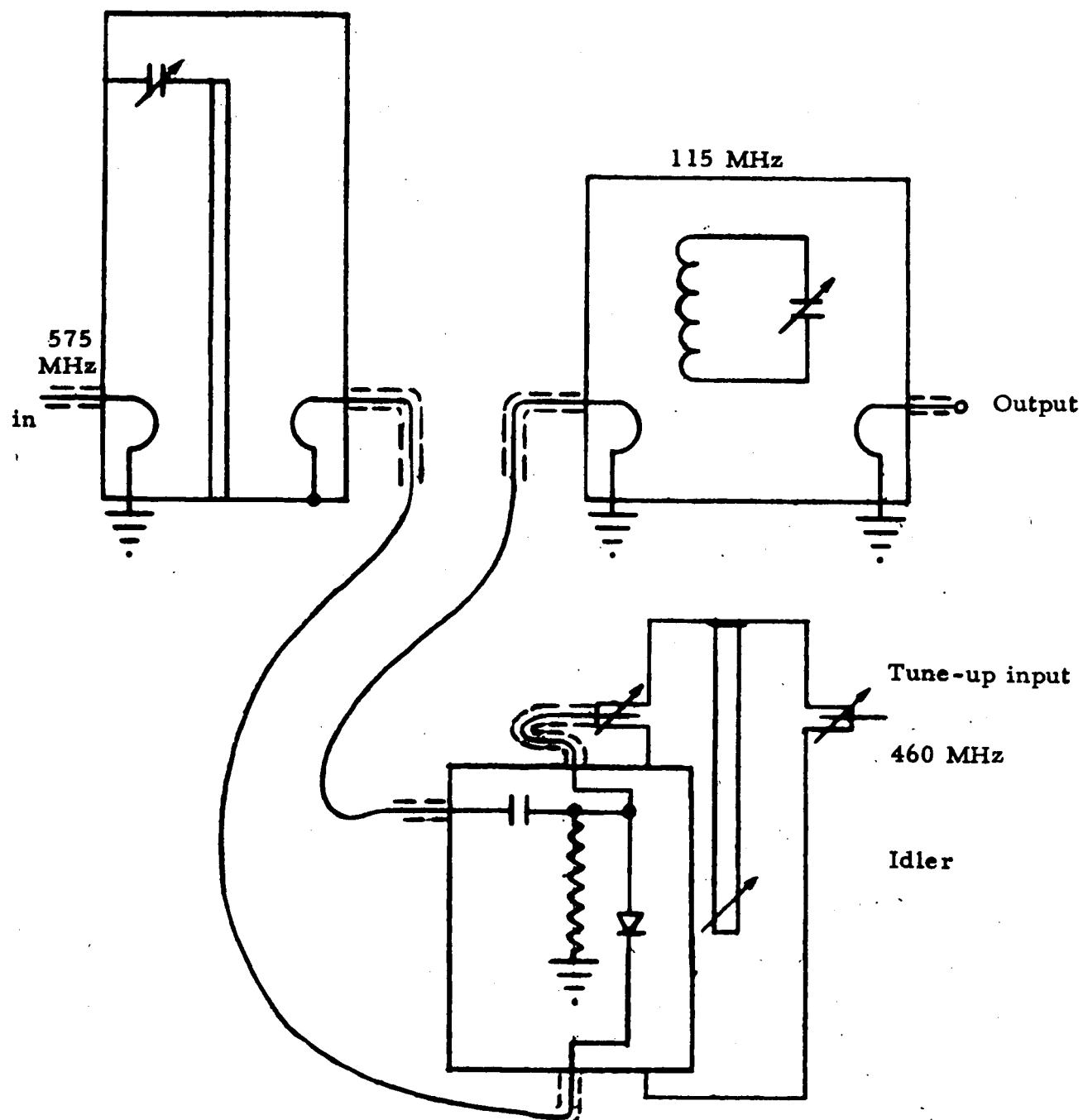115 MHz

Output

Tune-up input

460 MHz

Idler

FIG. 7   STEP-RECOVERY DIVIDER
EXPERIMENTAL SETUP

3)   Coincidence of a recurrent event of the complex waveform resulting from subharmonic, idler and input signals with diode transition may be an important factor in phase locking the three frequencies. Careful biasing may be required.

III.   MEASUREMENT OF PHASE STABILITY

During the period covered by this report, various commonly used approaches to the measurement of short-term stability have been reviewed and the significance of their readout considered. The effect of the frequency response of the measurement system on the readout of certain approaches has been of concern, particularly with regard to the system used at SEI for measuring phase stability.

A.   Survey of Measurement Schemes

Not all of the currently used short-term stability measurement systems have been reviewed, but rather those with possible implications in the area of phase stability. In recent years, considerable interest has been shown in various aspects of short-term stability and a number of worthwhile papers and articles presented. Representative papers will be found, for instance, in the Proceedings of the IEEE - NASA Symposium on Short-Term Stability (NASA SP-80). Those of interest here are principally those concerned with the time-domain, i.e. where the readout is in frequency or phase deviation in a given time interval rather than those dealing with the spectral distribution of energy.

1)   Balanced Mixer Methods

Two systems using balanced mixers in short-term stability measurement were reviewed. In one, the reference signal and the signal being measured are at the same frequency. This is essentially the method used in the measurement system utilized by SEI and will be treated later. The other is where the frequencies in question are dissimilar and a heterodyning operation occurs. In this case, the low resultant frequency is delivered to a wave analyzer and results in a plot of power per cycle versus frequency. This procedure may permit the identification of jitter due to some specific type of modulation.

2) Frequency - Discriminator Method

Mean-square frequency deviation, a commonly used measurement of short-term stability, can be obtained directly by use of a frequency discriminator, since its output is proportional to frequency deviation. The readout can then be specified for observation or averaging time by the use of filters having known characteristics.

3) Phase Measurement Systems

The balanced method in 1) above where identical frequency inputs are used is basically a phase measurement system, since the output of the mixer is a measure of the instantaneous phase difference between the input signals. Often this output is processed by differentiating to give an output proportional to frequency. The filtering system of 2) is then applied to this result to specify averaging time.

Elimination of the differentiating operation leaves a system where phase deviation is measured for a given averaging time. The system used by SEI has been of this type except that no deliberate filtering has been employed, but the equivalent cut-off frequency of the system, and therefore the limitations on averaging time, has simply been determined by component response, particularly the video amplifier response.

Figures 8 and 9 show the system used at SEI for measuring phase jitter contributed by a specific device, such as the fractional-frequency multiplier of Section IIB. This approach utilizes a common input signal to identical devices of the type to be tested. This permits a constant average guadrature relationship to be maintained at the two input channels of the phase comparator system.

This approach has been reviewed and the mathematical relationship simplified. This simplification results from the assumptions that, referring to the phase comparator of Fig. 9, the input signals are equal; the diode detectors are operated in a linear range; and the instantaneous phase deviation is small (less than $\pi/4$ rad.).
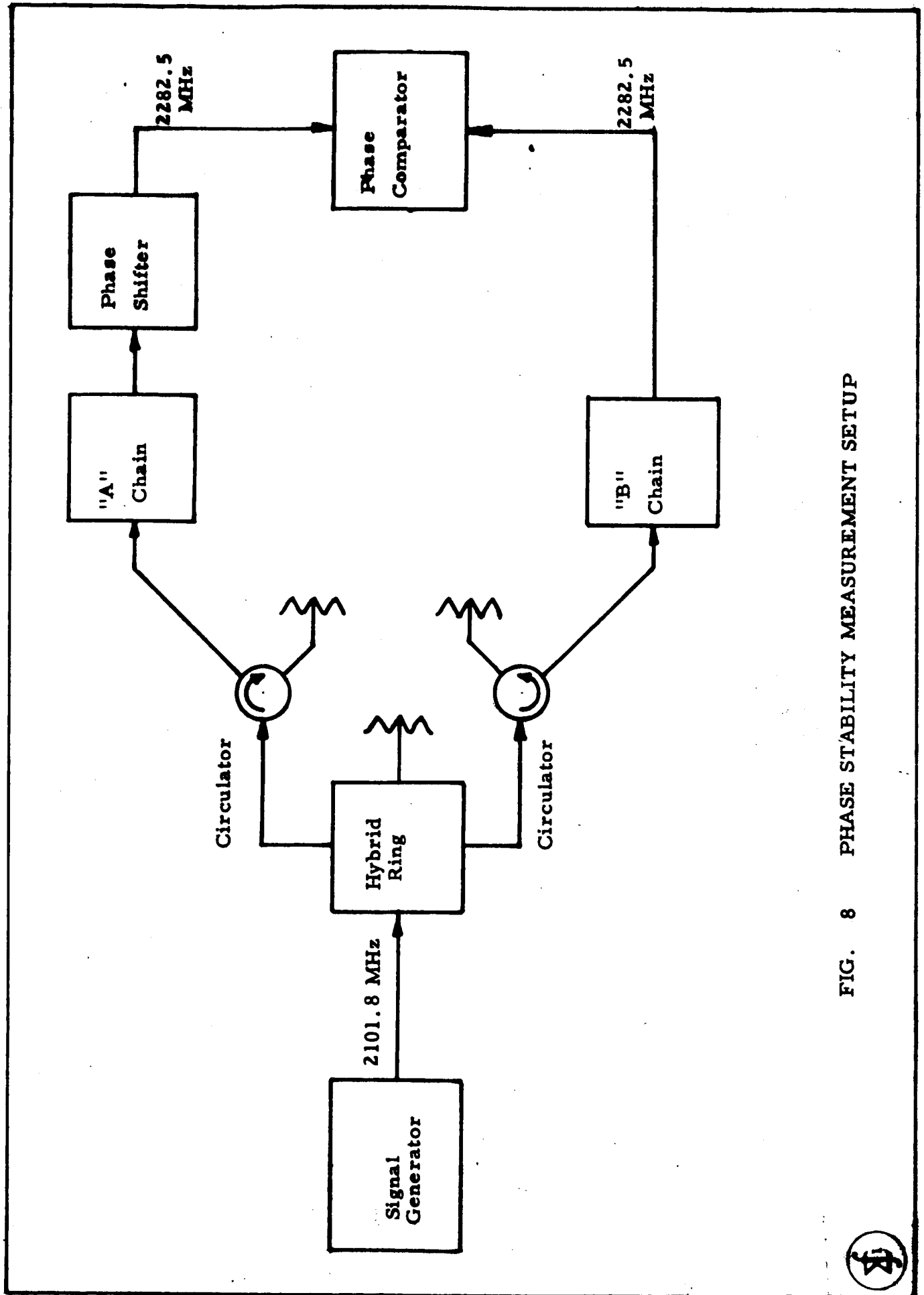
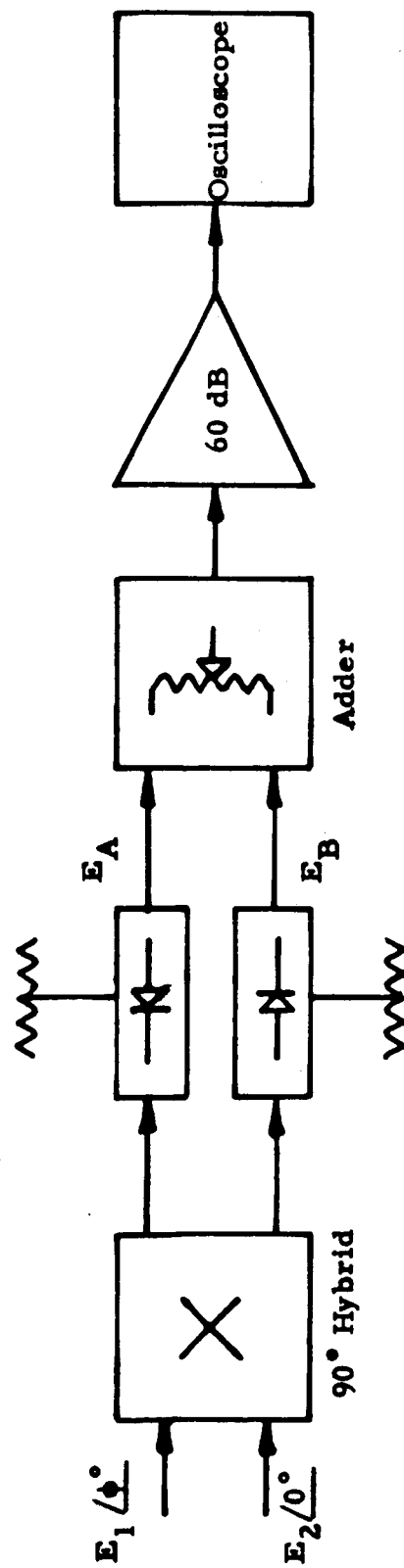FIG.   8   PHASE STABILITY MEASUREMENT SETUP

FIG. 9 • PHASE COMPARATOR

With a $90°$ hybrid as shown in Fig. 9, and with input signals of identical average frequency, but differing in phase as shown, the phase angle between the two signals emerging at one port will be $\phi - \frac{\pi}{2}$ and at the other port $\phi + \frac{\pi}{2}$.

Referring to Fig. 10, it will be seen that the assumption of equal magnitudes permits the magnitude of the resultant at one port to be written as

$$\left| E_A \right| = 2 E_1 \cos 1/2 \left(\phi - \frac{\pi}{2} \right) \tag{4}$$

Similarly for the other port,

$$\left| E_B \right| = 2 E_1 \cos 1/2 \left(\phi + \frac{\pi}{2} \right) = 2 E_1 \sin 1/2 \left(\phi - \frac{\pi}{2} \right) \tag{5}$$

Then, after diode rectification, the output of the adder will be

$$\frac{\left| E_A \right| - \left| E_B \right|}{2 E_1} = \left| \cos \frac{1}{2} \left(\phi + \frac{\pi}{2} \right) \right| - \left| \sin \frac{1}{2} \left(\phi - \frac{\pi}{2} \right) \right| \tag{6}$$

Here the magnitudes must be used because of the polarization due to rectification. Figure 11 is a plot of this result.

Consider the case where the average value of ϕ has been set at $\phi = \pi$ radians, i.e. where the slope in Fig. 11 is maximum and where the sensitivity is therefore greatest. This is also the point of zero dc output from the adder. Let $\phi = \pi + \Delta\phi$ where $\Delta\phi$ is an incremental phase error less than $\frac{\pi}{4}$ radians. Then

$$\frac{\left| E_A \right| - \left| E_B \right|}{2 E_1} = \left| \cos \frac{1}{2} \left(\Delta\phi + \frac{\pi}{2} \right) \right| - \left| \sin \frac{1}{2} \left(\Delta\phi + \frac{\pi}{2} \right) \right|$$

$$= \frac{1}{\sqrt{2}} \left| \cos \frac{\Delta\phi}{2} - \sin \frac{\Delta\phi}{2} \right| - \frac{1}{\sqrt{2}} \left| \cos \frac{\Delta\phi}{2} + \sin \frac{\Delta\phi}{2} \right| \tag{7}$$

E_1

E_A

E_1

$\phi - \pi/2$

$E_2 \, (= E_1)$
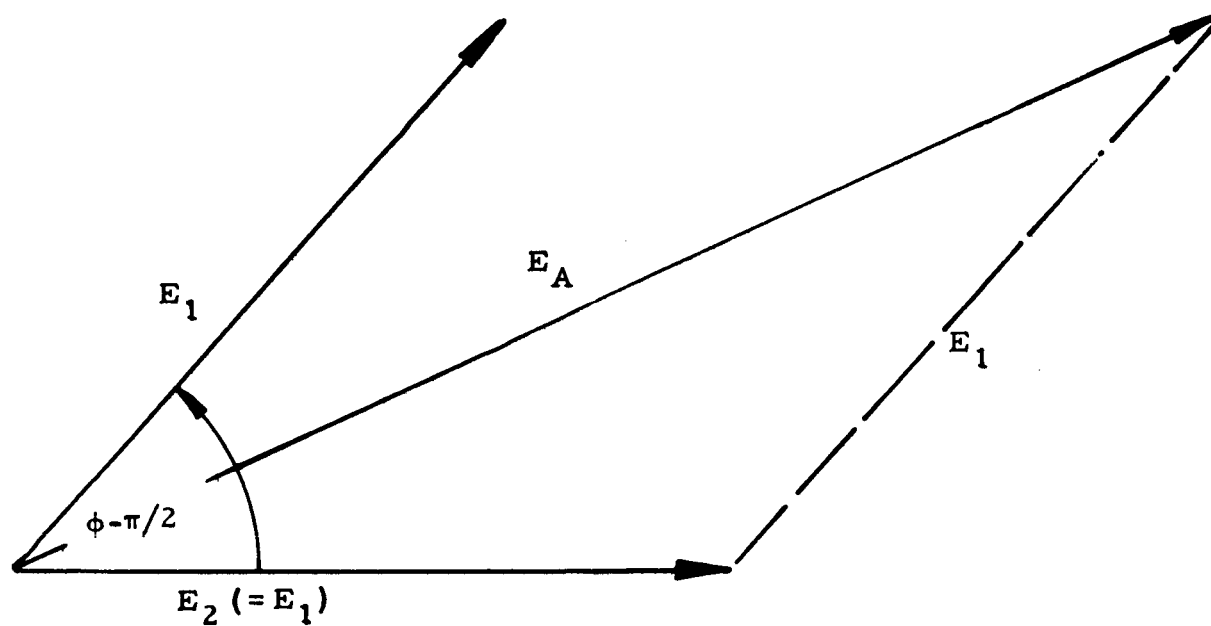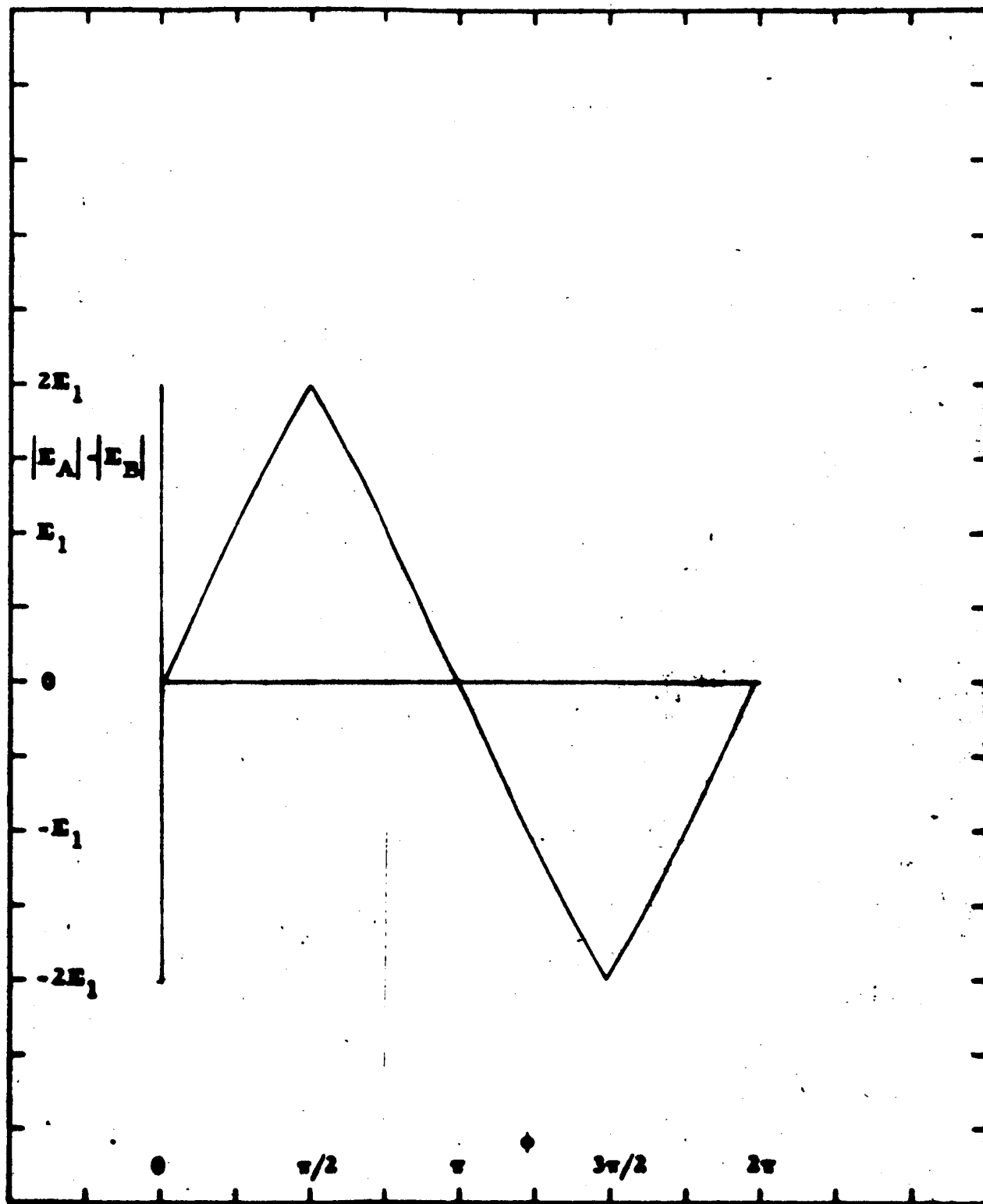
FIG. 10   VECTOR ADDITION OF PHASE COMPARATOR INPUTS

403A

FIG. 11 PHASE COMPARATOR OUTPUT VOLTAGE
vs INPUT PHASE DIFFERENCE (for $E_1 = E_2$)

Since $\Delta\phi \leq \frac{\pi}{4}$, $\Delta\frac{\phi}{2} \leq \frac{\pi}{8}$. Both bracketed terms will always be positive, and the absolute and algebraic values will be the same. Therefore

$$\frac{\left|E_A\right| - \left|E_B\right|}{\sqrt{2}\,E_1} = -2\,\sin\frac{\Delta\phi}{2} \tag{8}$$

Also $\sin\frac{\Delta\phi}{2} \cong \frac{\Delta\phi}{2}$ and

$$\frac{\left|E_A\right| - \left|E_B\right|}{\sqrt{2}\,E_1} \cong -\Delta\phi \tag{9}$$

The contribution of one of the devices under test, in the case of random phase noise will then be

$$\Delta\phi \cong -\frac{\left|E_A\right| - \left|E_B\right|}{2\,E_1} \tag{10}$$

In practice, the system is used as follows:

a) One of the inputs is removed and the adder balanced for zero dc output.

b) With both inputs connected, the phase shifter is adjusted for maximum dc output $(2\,E_1)$.

c) The phase shifter is then set for minimum dc output from the adder and the peak value of the video phase jitter read on the oscilloscope $\left(\left|E_A\right| - \left|E_B\right|\right)$.

The effect of the system frequency response has been considered. Because of the bandwidth of the video amplifier, which is the limiting factor in the system, high frequency components of phase jitter will be somewhat attenuated. However, it is felt that the pass band is adequate for reasonably accurate measurement of the significant components of phase noise.

IV. RECOMMENDATIONS

As a result of the work on Contract NAS 8-11592, several areas of interest have emerged and SEI recommends that the following items be considered for future investigation.

A. Continuation of the theoretical analysis using the proposed audio frequency model of the step-recovery diode.

B. Experimental investigation of the possibility of high effeciency, low noise up-and down-conversion with step-recovery diodes.

C. Investigate the possibility of employing hybrid combinations of tunnel-diodes and step-recovery diodes in high efficiency frequency changers.

A proposal has been submitted to Marshall Space Flight Center by SEI to conduct the above investigations.